SOI Design in Cell Processor and Beyond

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Abstract—A brief historical overview of the microelectronics of the present home entertainment LSI chips with regard to the product specifications and performance aspects of the home entertainment LSI chip sets, such as for digital cameras, home robotics and games are given in order to explore the possible killer applications as our driving force for our future semiconductor and electrical and electronic industries. SOI design in Cell Processor is one good example. But some further technology break-through may be needed for our future potential real-time AIPS/AINS applications. Here, AIPS stands for Artificial Intelligent Partner Systems and AINS stands for Artificial Intelligent Nursery Systems.

I. INTRODUCTION

This talk is actually a continuation or the second part of the presentation delivered by the author at the ESSCIRC2001, which was held in Vilach Austria in September 18-20 2001 [1] Due to events of 11 September, the author could not attend in person, but his presentation via a conference connection was exemplary and well received.

At that presentation, a brief historical overview of a first home entertainment consumer electronic gadget, called a portable transistor radio was given, and then some introductory comments on the basic semiconductor device concepts were explained. They were strongly related to the microelectronics of the present home entertainment LSI chips with regard to the product specifications and performance aspects of the home entertainment LSI chip sets, such as for digital cameras, mobiles, and games.

Seven years have passed since then and surely these evolving modern electronic gadgets surely have changed our life and style drastically, but the consumers are demanding always, still better performance and quality. The semiconductor and electrical and electronic industries have drastically transformed their status for the customers' needs in their surviving games.

There were many merging and immerging companies in order to provide swiftly for the consumers better products with better performance and quality. It is very important to find out what the consumers really want, and much more important to supply what they really want as soon as possible or at least in time. Yes, sometimes, it is very hard to predict what the consumers really want.

Too early introduction to the consumer market may cause some critical damage or discouragements for the future product planning and development. However, it is worth trying ASAP to challenge to see the feasibility of a new methodology or a choice of technology to realize the desired product specifications and performance aspects of a new revolutionizing home entertainment gadget.

Bipolar Transistor Technology is one example that accelerated the portable radio consumer market in 1950s. CCD Technology is another example that accelerated the portable video and digital cameras in 1980s. SOI Design in Cell Processor [2] could be considered as another challenge to revolutionize the consumer semiconductor technology that has been proved to be successfully adopted for the mass-production just in time for customers' needs.

The Bipolar technology, the CCD technology and the SOI technology will surely contribute for the future consumers' specific high-class products for many, many years to come, and the real profit may lie in these devices enjoyed by a limited number of semiconductor vendors who have accumulated many year's production experience and know-how while the CMOS Logic LSI Chips Technology, the CMOS Imager Technology, and the CMOS Bulk Technology for future Multi-core processors may be well standardized and utilized for low-cost and low-profit products, but serving for a huge consumer market segment.

Our future is not ours to see. Whatever will be will be, but some insight and future prospective may be possible if the future killer application can be clear in picture with well-defined product specifications and performance aspects of a new revolutionizing home entertainment gadget for our future mass-production consumer business enhancement.

Some further technology breakthrough may be needed for our future potential real-time AIPS/AINS applications. Here, AIPS stands for Artificial Intelligent Partner Systems and AINS stands for Artificial Intelligent Nursery Systems.

II. BIPOLAR AND MOS DESIGNS

A small portable radio called TR-1 in Regency brand was being sold in Liberty Music Store in New York City for the price of \$49.95 during the December Christmas holiday season in 1954. It was seven years after the invention of the bipolar transistor in December 1947.

The radio is made of four n-p-n grown-type Bipolar Transistors with the 22.5 volt stacked type 015N battery being used in US Army. The picture of the TR-1 Regency brand Radio and its Circuit Diagram are shown in Fig.1a and Fig1b. below .



Figure 1 a

Regency TR-1 Radio

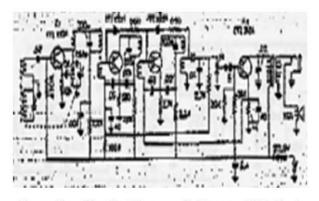


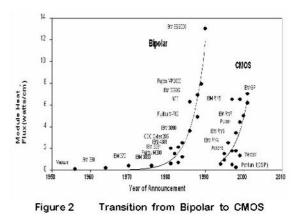
Figure 1b Circuits Diagram of Regency TR-1 Radio

However only ten thousand units were produced due to the poor reliability and high cost. The problem is that the transistor has a very low internal impedance and it needs a high by-pass capacitor of a few micro-farads. The transistor itself had a very low yield these days.

A small venture company in the far east conquered these problems and introduced the world most reliable and compact consumer TR-55 portable radio with 6 volt supply voltage in Aug 20, 1955.

More than fifty years have passed, but many innovative RF and Wireless papers with integrated capacitors and inductors are still high lighted in the international technical conferences and being implemented in real consumer products.

Though we see the transition from Bipolar to CMOS in many applications such as the one shown in Figure 2 below, the analog , wireless and RF circuits are still holding important roles in our semiconductor industry.



III. CCD AND CMOS IMAGER DESIGNS.

The basic pinned-diode structures adopted for the sensor elements both in CCD imagers and CMOS imagers are identical. The original structure was proposed by the author in 1975 and now it is a free patent[3][4][6]. The original idea came from the floating and lightly-doped base n-region utilized as the photo-electrons dynamic storage area in a conventional but slightly modified p-n-p bipolar junction transistor embedded in the n-substrate. This structure was the basic of the most of the universally adopted sensor elements in CCD and CMOS solid-state imagers now a day. Figure 3 below shows the structure

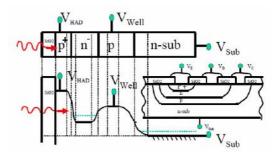


Figure 3 p-n-p-n Sensor Structure for CCD&CMOS Imagers

The relatively highly-doped emitter region quenched the undesired electric field at the Silicon SiO2 interface, and very low dark current and defect free image sensing element was realized. More over even though this is very similar to the p-np bipolar transistor structure with n-type substrate, the p-n-p transistor operates dynamically with the base storage junction capacitor region floating. With this structure one single photo detection may be possible when the lightly doped floating base is depleted completed. The same floating lightly doped base BJT sensor elements can be utilized both in the CCD imager in Figure 4a and in the MOS imager case as seen in Figure 4b below.

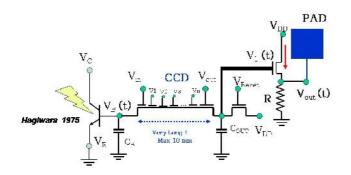


Figure 4a CCD Imager with Floating-Base BJT Sensors with Vertical and Horizontal CCD Shift Registers

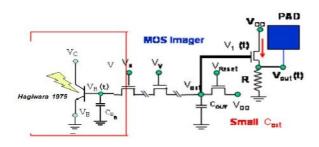


Figure 4b The Same Floating-Base BJT Sensor with CMOS X and Y Transfer lines in CMOS Imager

Here we observe that even in CCD Imagers the output circuits are made of the CMOS source-follower circuits. And even in the CMOS imager case, the basic sensor element is the basic BJT sensor structure. Even a pinned diode, it is a p-n-p structure. A variety of technologies are all incorporated and utilized to achieve the best device performance.

IV. CMOS BULK AND SOI DESIGNS

Ten years has passed after the introduction of SOI into a product. Was SOI considered as a competitor to bulk CMOS then ? Now we see both technologies continue to co-exit in some of the application domains, such as microprocessors and gaming.

However, we also see the exclusive use of bulk CMOS in main stream SOC. It was thought 10 years ago that SOI has

a performance advantage over bulk, and the cost would be its barrier for wide application. In this speculatives no one was sure about what were the applications. There were no clear pictures of the killer applications except PC and game processors in the huge consumer markets.

Figure 5 Two Technologies Overview

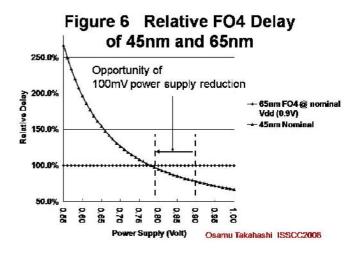
| Osamu Takahashi ISSCC2008 Technology | | 65nm SOI CMOS Technology on p- SOI Substrate | 45nm SOI CMOS Technology on p- SOI Substrate | Scaling | | | | | |
|---|--------------|--|---|--------------|----------------|--|-----------------------|-----------------------|---------------------|
| Used | Thin Ox Hvt | yes | yes | | | | | | |
| Device | Thin Ox Rvt | yes | yes | | | | | | |
| Туре | Thick Ox Rvt | yes | yes | | | | | | |
| Thin Ox Tox | | 1.12 nm | 1.16 nm | | | | | | |
| Thick Ox Tox Nominal Supply (Thin Ox) Nominal Supply (Thick Ox) M1 Minimum Width M1 Minimum Spacing | | 2.35 nm 1.0 V 1.5 V 0.1* um 0.1* um | 2.50 nm 0.9-1.0 V 1.5-1.8 V 0.076* um 0.076* um | 0.76 0.76 | | | | | |
| | | | | | Metal Layers | | 10 | 16 | , |
| | | | | | SRAM Cell Area | | 0.700 um ² | 0.404 um ² | (0.76) ² |

Cell/B.E. design specific. Not technology specific

Since most of the circuits engineers are working on bulk-CMOS chips, before comparing or discussing about the features of BulK and SOI CMOS, the basics of SOI needs to be understand.

Figures 5 thru 7 give some good insights of SOI performance. Obviously, there are specific performance requirements from graphics/games processors. Some specifics of the technology used in the CELL processor must be understood.

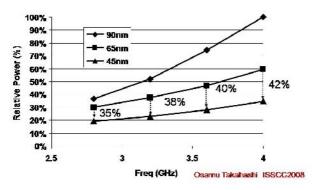
It would be of general interest to learn about new design and library techniques - challenges faced, new solutions, how technology features are exploited and what has been achieved. Then we can really discuss on why do it, and about the key issues.



V. CELL PROCESSOR

Ken Kutaragi[5] in his plenary talk "The future of computing for real-time entertainment", at ISSCC2006, February 2006 started with a short review of computing and computer games, from Eniac, through microprocessors and text-based games, to Pong, and now approaching real-time computer generated graphics.

Figure 7 Simulated Relative Power of Cell/B.E. with Three Technologies



This trend is continuing, expanding the market from homes and fixed-location gaming, to the mobile space. This trend will increase IC content and push the limits of the semiconductor processes. In the early games, the game platforms used mature technologies like TTL, so the internal silicon was always one or two generations back from the leading edge. The gaming market was fairly small and most games were just advanced toys. Designs were integrated into ASICs to reduce costs and size, but there was no effort to push the technology.

Figure 8 45nm Cell/B.E. Die Photo

Osamu Takahashi ISSCC2008

By 1994, the games were just starting to move to 0.5-micron processes, while the leading process was 0.35 micron. Eventually over time, the game chips migrated to smaller processes to increase integration and reduce costs. Now games

are a big business, Over 700 million gaming platforms are in players' hands, and the industry consumes 70,000 8-inch wafers per month for logic and memory – with demand increasing in 2007 to over 120,000 8-and 12-inch wafers per month. The latest games are multi-core SoC devices that push the state of the art in semiconductors.

The PlayStation became one of the first gaming systems to push the technology. It is similar in architecture to a PC, except for its MIPS processor and dedicated geometry transfer engine. Due to the 5-stage pipeline in the graphics chip, the latency approached 100 msec – a speed that humans discern as discontinuous and definitely not real time.

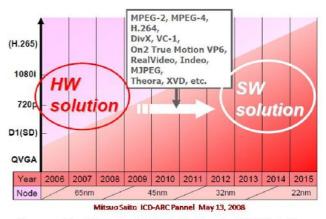


Figure 9 Trend of HW Solution to SW Solution

To address the latency issue, the emotion engine was developed in 1998. This groundbreaking graphics chip needed the latest technologies to achieve its performance and level of integration. By reducing the number of pipeline stages and increasing integration – with 10.5 million transistor and a 128bit dual vector processor – the Playstation pushed all of the existing limits of the 250-nanometer process.

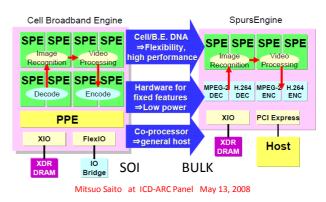


Figure 10 Cell/B.E. and Toshiba SpursEngine

In 1999, the design was ported to a 4-metal, 180-nanometer process to reduce size and increase performance. The following year, it was ported to a 130-nanometer process. The 2-chip set was reduced to a single chip in a 90-nanometer process in 2004.

Also in 2004, the portable PSP platform was introduced. This gaming system uses a 9-metal, 90-nanometer process and has 18 million transistors in a multi-core architecture. The advent of real-time response in games changed the entire experience. Just as computers changed lives by bringing new compute capabilities to the office – first through spreadsheets, then communications and publishing, and finally to the rest of the high-technology lifestyle through video and music – the new games brought other changes.

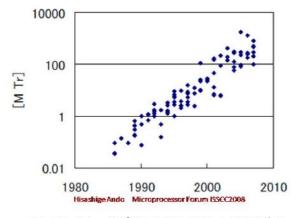


Figure 11 # of Transistors on a MPU chip

Real-time response now allows the user to interact more closely with the games. The absence of any noticeable lag immerses the user in the action. The need for more computing and massive I/O capabilities is acknowledged in any real-time situation.

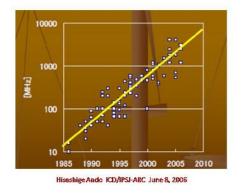


Figure 12 Trend of Processor in ISSCC papers

For example, a Formula 1 car has over 200 sensors and needs a supercomputer to process the data in the time available. Other real-time applications have similar requirements. The real-time environment forces the computer designer to change from a storage-centric to a processing centric model, with low latency and high throughput as essential design characteristics.

The Cell chip is a very highly parallel, multi-core processor with massive bandwidth for memory and I/O. Among the new capabilities in the chip are internal hardware security functions and an architecture geared for high scalability. Figure 8 shows the current 45 nm Cell Processor.

The Cell chip represents the convergence of supercomputers and computer entertainment in massively parallel systems with real-time response, quickly approaching the prospect of a super artificial intelligence that includes vision systems, intelligence – and even curiosity, as we saw in HAL in the film 2001.

The weight on the software developments efforts will be much heavier and heavier in near future. See Figure 9 above. We also see now SOI and Bulk co-exist in variety of differenct unique applications. See Figure 10.



Ref: http://www.top500.org Figure 13 Projected Performance Development

Next-generation systems will include not only the supercomputers as explained in Figures 11 thru 13, but also vast number of sensors of all types to change the way humans and computers interact. Game machines have gone from trailing-edge components to leading-edge SoC devices over the past 30 years. But Game machines are not the only real-time applications. There must be more potential applications of real real-time machines in order to meet our human needs.

The future of real-time computing will include massive assemblies of parallel processors over mesh-connected networks to execute the vast amounts of computation that recognize and react to the real world with many types of sensors and interface and networking connections.

The enhanced capabilities of the supercomputer-class devices will change user experiences and expectations in ways we are not fully aware of and not able to define, at least for now. Face recognition and real-time cosmetic face simulation can be realized with dedicated processors. SpursEngine by Toshiba is one good example. See Figure 10 above.

But the real killer application may be just waiting at the corner to appear in front of us suddenly soon. Since the need is the mother of inventions, all we need to look for is just what we really wish to have in our daily life at home and outdoors.

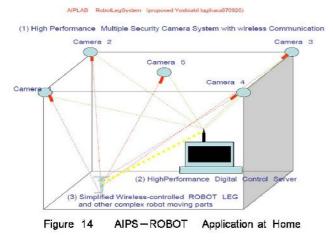
VI. AIPS/AINS-ROBOT APPLICATIONS

The author believes the key lies in the human friendly AIPS and AINS-Robot Applications. A robot is a product of many technology achievements including material science, mechanical engineering, electrical engineering and a huge amount of supporting software environments with real-time supercomputers and communication wire-line and wireless networking.

If the robot application is dedicated for the daily care of old and disabled people at home, the dedicated AIPS/AINS system also needs to consider the barrier free house design efforts and for the natural friendly human-robot interface, the human-friendly robot appearance and cloths are desired.

The convergence of supercomputers and computer entertainment in massively parallel systems with real-time response, quickly approaching the prospect of a super artificial intelligence that includes vision systems, intelligence – and even curiosity, as we saw in HAL in the film 2001.

Next-generation systems will include vast number of sensors of all types to change the way humans and computers interact.



At home, every room has many, many sensing video cameras and audio sound pick-up systems wired together in the home network system with the super computers processing the voice and image pattern recognitions in real time, and the advanced AIPS/AINS Software will control the robust mechanical robot arms, legs and moving wheels to respond in real time to the requirements and requests given by the old and disabled people at home.

Current humanoid robots are being designed to be mobile and portability-oriented design with many constraints in power management and body-space limitations.

But by sharing a variety of functions with in- door furniture-type TV display super computer terminal, internet remote control intelligent services, toy-type sensors, the mechanical robot body itself can be designed and dedicated to achieve fully- reliable and accurate human-like gentle and strong movements.

What we really needs is the total computer controlled robot system that can really control in real-time the complicated mechanical system such as the One-legged Ghost Umbrella Toy or the Classical Japanese Johruri Doll Play.



(3) a computer-controlled new version of the Classical Japanese Bunraku Doll Theatre System.



http://www2.ntj.jac.go.jp/unesco/bunraku/jp/contents/whats/index.html

Figure 15 Another AIPS/AINS-ROBOT Application Images

These systems can be achieved with the real-time feedback systems with many video camera and audio pick-up interfaces.

The entire system may be connected to the established security service company or privately connected to their children and wives outside home by mobile phone and wireless real-time communication system so that the old and disabled people need not be cared and confined in the remote hospital away from their family and friends. With the dedicated their own private AIPS/AINS-Robot services, the old people's daily care nursery home may not be important for them.. They can stay at home with their children, grandchildren and friends and family for the rest of their lives happy after.

While the person is still active and clear in mind, the AIPS-Robot serves as the real partner friend to them. They can teach or program the AIPS-Robot as they wish with many dedicated hours for their own dedicated requirements.

When the people gets old, forgettable, and disabled, the AIPS-Robot can work continuously now as the AINS-Robot as a friend to the old and disabled man. These applications can be realized with the super-computing processors, video camera and audio sound sensing systems all connected and effectively with wire-line wireless real-time communication channels, also with the comfortable display screen and audio-sound track systems built-in at home. Since the day-care home service system for the old and disabled people can be defined quite accurately, the system requirements and specifications can be well defined. The entire system can be also achieved in a much larger scale in outdoors. Maybe what we need is only one supercomputer or one big network of supercomputers all connected in one to act as one entity in super real-time. All the AIPS/AINS-robots can be assisted to perform natural way serve people.

VII. CONCLUSION

In ISSCC2006, Ken Kutaragi talked his vision on the future of computing for real-time entertainment in details. Almost three years have passed since then. And now the PS3 game consoles with blue-ray disk and SOI-CELL Processor are now in the hands of the consumer market in the stage of the full enjoyment of mass production. Time is now ready for us to see the real real-time applications, more functions with the full supports of the game machine capability, supporting the virtual-world entertainment applications. We now look for more than the simple real real-world applications such as the game-robots and the Robo-Cups. The real killer application is what the mass consumer market is waiting for.

The author believes that the target application is the completely human-friendly AIPS/AINS-robot total service system solution at home. To achieve this, goal, the semiconductor engineers, electrical and electronic engineers, software engineers, mechanical engineers, house-designers, even the garments fashion-clothes designers and art designers must work together hands in hands.

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AIPS = Artificial Intelligent Partner Systems.

AINS= Artificial Intelligent Nursery Systems.

See http://www.aiplab.com/

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